Acube Portable Mother Board Bring-up Technical Report

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1 Document Control

Title:	Acube Portable Mother Board Bring-up Technical Report
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1.1 Revision history

Revision	Date	Author	Notes
1.0	05/04/2025		Initial version

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2 Abstract

This document summarizes the findings from the analysis of the bring-up process of the “Acube Portable” board (*the board*). *The board* is a custom system built around the NXP QorIQ T2080, a 4-core PowerPC64 CPU. Several errors were discovered during the schematic review. The system was able to partially boot, but not to a usable state.

3 Introduction

The primary objective of this analysis was to boot U-Boot on the board as a preliminary step toward running a full Linux distribution. Tests were performed on the board with serial number 210921A.

The board was powered by a bench-top power supply providing 12V at a maximum of 5A. Tests were conducted without any SODIMM module installed and with a microSD (µSD) card used as the boot source.

A USB-to-serial adapter (RS232 levels) was connected to the serial port header J9.

A CodeWarrior TAP JTAG interface, used in conjunction with the CodeWarrior IDE, was employed to debug the system. A custom cable adapted from a 2x8 2.54mm connector (probe side) to a 2x8 2mm connector (board side, J3) was used.

An FTDI C232HM-DDHSL-0 cable was used to program the on-board CPLD via header J10, using Lattice Diamond. A development kit (T2080RDB rev. C) served as a reference system to validate the µSD boot process.

4 Reference Documents

- QorIQ T2080 Data Sheet (NXP account required)
- QorIQ T2080 Design Checklist
- QorIQ T2080 Reference Manual (NXP account required)

5 Glossary

- **DNP**: Do Not Populate
- **PBI**: Pre-Bootloader Instructions
- **PBL**: Pre-Bootloader
- **PORESET**: Power-On Reset
- **RCW**: Reset Configuration Words

6 Brief Boot Sequence Explanation

Note: This section provides an overview of the T2080 power-on and boot process. For more details, refer to T2080RM section *4.6.1 Power-On Reset Sequence*, T2080 section *3.2 Power Sequencing*, and T2080RM chapter *5 Pre-Boot Loader (PBL)*.

After a successful power-on sequence, the *Pre-Bootloader* (PBL) samples the Power-On Configuration Signals. Among other things, these signals determine the boot source:

cfg_rcw_src[0:8]	Source
0_0010_0111	NOR Flash
0_0100_0000	SD Card
0_0100_0101	SPI Flash
1_0001_1001	NAND Flash

The boot source can be changed using the SW1 and SW2 DIP switches.

Once the boot source is selected, the PBL loads the Reset Configuration Words (RCW) from the chosen boot media to configure the platform. If the RCW sets PBI_SRC, the Pre-Bootloader Instructions (PBI) are also loaded form the µSD and executed.

After PBI execution, the PBL searches for the main application — in this case, u-boot-spl — in the selected boot media.

Summary of the Boot Process:

1. The PBL samples the Power-On Configuration Signals.
2. It loads the RCW from the boot media.
3. If configured, it executes the PBI.
4. It loads the main application (e.g., u-boot-spl).

7 U-Boot

A microSD card was flashed with mainline U-Boot, compiled on Ubuntu 24.04 using the 32-bit PowerPC toolchain. The source was obtained from denex u-boot repo using tag v2024.10. The default configuration T2080RDB_SDCARD_defconfig was used.

The final binary, which includes PBI, RCW, and U-Boot, was written to a 2GB

microSD card using:

dd if=u-boot-with-spl-pbl.bin of=/dev/mmcblk0 bs=512 seek=8

To enable the CLK_OUT pad, the following line was appended to the PBI source file t2080_pbi.cfg:

090E1A00 0001CE00

This configuration:

- Enables the CLK_OUT signal
- Selects the platform clock divided by 3 as the source
- Applies an additional divide-by-8

See CLK_OUT Test for measurement results.

The µSD card was validated on the T2080RDB development kit.

It is worth noting that the compiled U-Boot image targets the T2080RDB platform, which features a different hardware configuration (CPLD, co-processor, GPIOs, etc.). However, the SPL portion of U-Boot is sufficiently hardware-agnostic to run on the CPU without requiring modifications.

8 CLK_OUT Test

For more information, see T2080RM section 4.5.4. and note that the CLK_OUT pad is not routed; to probe it, a fanout via was exposed and a wire was soldered to it.

8.1 Clock Sources

- Platform Clock ÷3
- Platform Clock ÷4
- Platform Clock ÷2
- Platform Clock ÷1
- Platform Feedback Clock
- SYSCLK

8.2 Divider Options

- ÷1
- ÷2
- ÷4
- ÷8

The Clocking_CLKPCSR register controls the CLK_OUT pad. Configuration was written via the PBI file (see U-Boot). The CPU reference clock runs at 66.7 MHz.

8.3 Divider Options

8.3.1 Measurement 1: SYSCLK:Platform Clock Ratio = 1:6 (RCW[SYS_PLL_RAT] = 0b0_0110)

- Platform Clock = 66.7MHz × 6 = 400MHz
- CLK_OUT = 400MHz ÷ 3 ÷ 8 ≈ **16.7MHz**
- See figure 1

8.3.2 Measurement 2: SYSCLK:Platform Clock Ratio = 1:8 (RCW[SYS_PLL_RAT] = 0b0_1000)

- Platform Clock = 66.7MHz × 8 = 534MHz
- CLK_OUT = 534MHz ÷ 3 ÷ 8 ≈ **22.2MHz**
- See figure 2

Figure 1. CLK_OUT 6:1 400MHz

Figure 2. CLK_OUT 8:1 535MHz

9 CPLD

The following signals involved in the PORESET sequence were analyzed:

SIGNAL	DIRECTION (CPU)	FUNCTION
PORESET_B	Input	Triggers the power-on reset sequence
HRESET_B	Input/Output	Asserted by CPU at PORESET; also used externally
RESET_REQ_B	Output	
TRST_B	Input	

In the current CPLD firmware, PORESET_B is misconfigured as a push-pull output. Since the CPLD operates at 3.3V and the PORESET_B line is externally pulled to 1.8V (via R79), the CPLD should drive this signal as open-drain. HRESET_B is correctly configured as open-drain and pulled to 1.8V via R78.

10 JTAG

The JTAG interface is only partially implemented. AN4804 Figure 3 describes the expected JTAG wiring.

In the custom design:

- COP_HRESET_B and COP_SRESET_B are not routed.
- COP_TRST_B is connected directly to the CPU and pulled to 3.3V (should be 1.8V).
- J3-5 is shorted to J3-11.

A workaround was attempted to replicate the AN4804 setup:

- Removed R123, R285, R287, R291, R293
- Repurposed CPLD pins and rewired JTAG signals to match the reference
- Updated CPLD firmware to handle new signal mapping

Despite these changes, the JTAG attach operation still failed.

11 T2080RDB Comparison

The PORESET sequence was compared between the custom board and the T2080RDB.

The board meets the required assertion time of at least one 1ms for PORESET_B, as seen in figure 3.

However, the T2080RDB shows a spike ~40ms after trigger, with an assertion time of only ~225ns, as shown in figure 4 with a detailed view in figure 5.

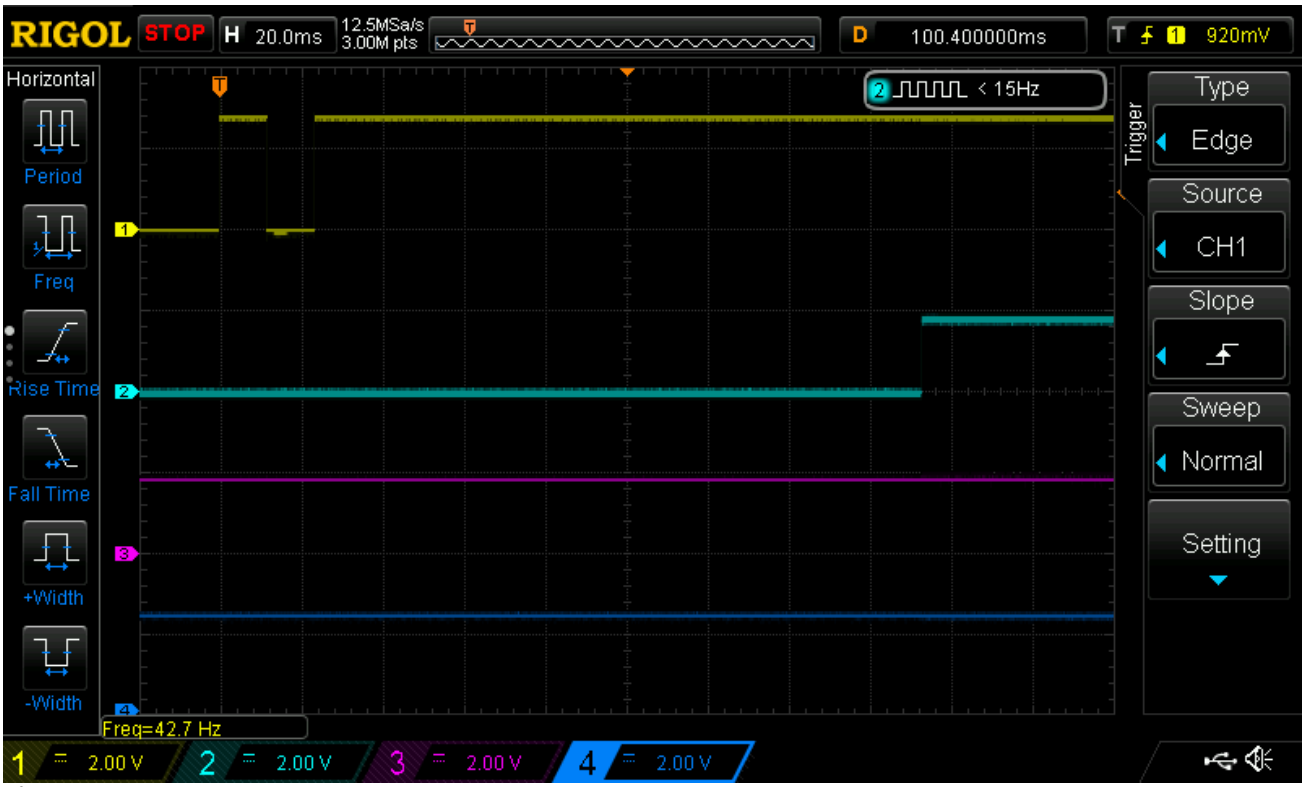

Figure 3: Board PORESET sequence

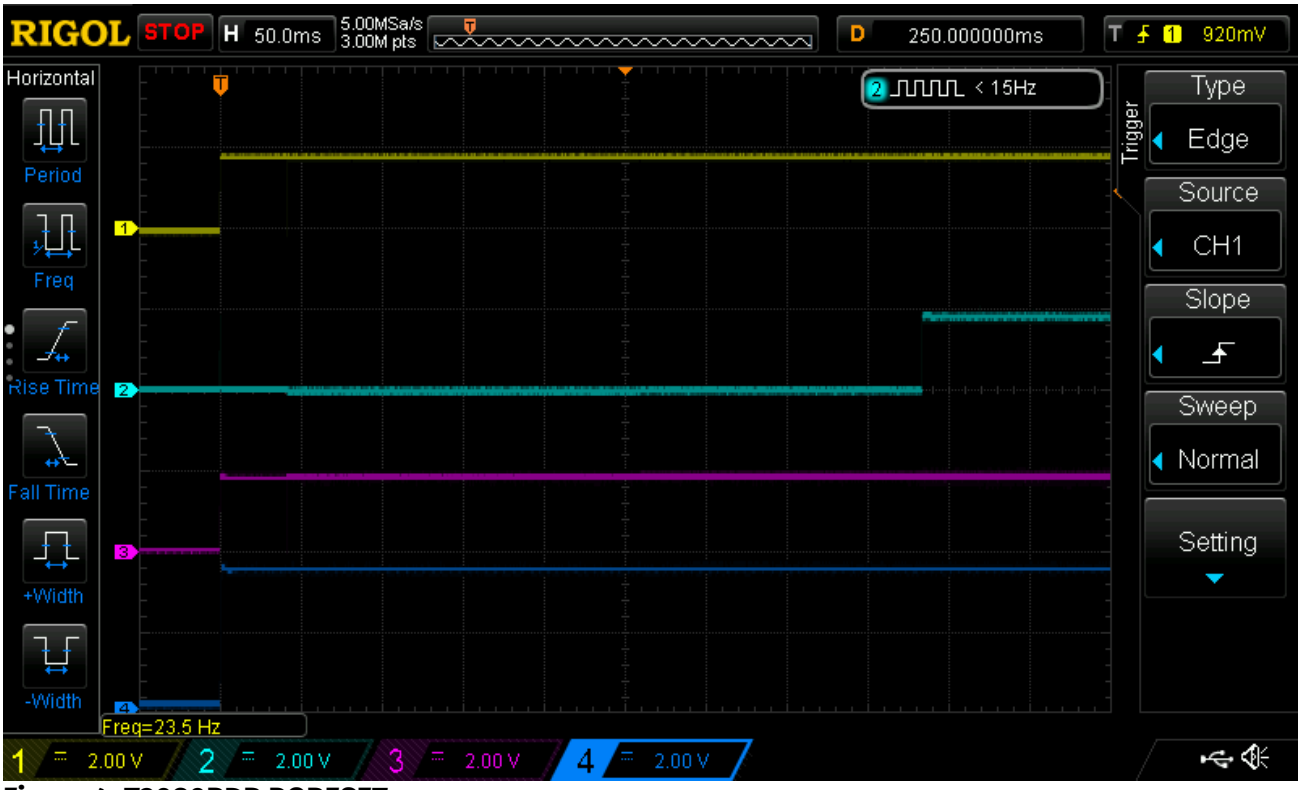

Figure 4: T2080RDB PORESET sequence

Figure 5: Zoomed view

HRESET_B is held low for ~400ms on the T2080RDB vs. ~150ms on the custom board.

12 Hardware Review

Schematic version 0.5 (PDF link) was reviewed.

12.1 Issues Found

- PROG_MTR and FA_VL must be pulled to GND (they are reserved). R375 and R379 should not be populated.
- PROG_SFP must be pulled to GND during normal operation. R377 should not be populated.

12.2 DNP Discrepancies

The following components are marked DNP on T2080RDB but are populated on the custom board:

Designator(s)	**Notes**
R23	Pull-down on IFC_A20 — must not be pulled low at POR
R73	Pull-up on SDHC_WP
R707, R708, R715, R710, R717, R718, R723, R724, R728, R729, R732	Pull-downs on PCIe clock generator outputs
R720	Spread selector on PCIe clock generator
C91	Capacitor on EC1_GTX_CLK
C121, R192	Snubber on USB_IBIAS_REXT
C126	Capacitor on USB_REFCLK
C803, C809	Capacitors on SYS_REFCLK and DDR_REFCLK
FUSE1	Fan fuse

12.3 HW verification

- PCBA integrity checking revealed no evident problems except the manual patches done by MAS Elettronica with no documentation provided
- primary and secondary Power Rails of the custom board were verified with positive results (U65, U73 to U75, U76, U77, U90 to U95)
- JTAG port connections are not compliant to the RM and a short between two signals is found (refer to p.10)

13 Conclusions

Although several issues were identified and addressed, the board still fails to boot U-Boot successfully.

Partial boot functionality is confirmed (see CLK_OUT Test).

JTAG download works using the CodeWarrior-generated application, but JTAG attach remains non-functional on the custom board, even after hardware modifications — unlike the T2080RDB, where JTAG attach works reliably.